



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,570	01/20/2004	Takahiko Murata	60188-754	8016

7590 12/09/2009
Jack Q. Lever, Jr.
McDERMOTT, WILL & EMERY
600 Thirteenth Street, N.W.
Washington, DC 20005-3096

EXAMINER

CUTLER, ALBERT H

ART UNIT	PAPER NUMBER
----------	--------------

2622

MAIL DATE	DELIVERY MODE
-----------	---------------

12/09/2009

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/759,570	Applicant(s) MURATA ET AL.	
	Examiner ALBERT H. CUTLER	Art Unit 2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 September 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 4,5,12,14-23 and 25-38 is/are pending in the application.
- 4a) Of the above claim(s) 4,12,14,16,17,20,22,25-27 and 31-34 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 5,18,19,21,23,28-30 and 35-38 is/are rejected.
- 7) ☒ Claim(s) 15 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This office action is responsive to communication filed on September 17, 2009.

Response to Arguments

2. Applicant's arguments filed September 17, 2009 with respect to claims 5 and 35 have been fully considered but they are not persuasive.

3. Applicant argues, with respect to claim 5, that Umeda fails to describe or suggest a solid state imaging apparatus that includes, among other features, a signal output circuit configured to perform one of two types of operations, wherein in both of the first and second signal transmission methods, each of the selection signals of the shift register is output via the operation switching circuit to a corresponding pixel included in a pixel group arranged in the same direction as the shift register, such that all pixels in the pixel group receive a selection signal from the shift register. Applicant argues that in Umeda sub-sampling of pixel data is performed, and that in the present invention sub-sampling is not performed.

4. The Examiner respectfully disagrees. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., that sub-sampling of pixel data is not performed in either of the two signal transmission methods) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Claim 5 recites "wherein in both of the first and second signal transmission methods, each of the selection signals of the shift

Art Unit: 2622

register is output via the operation switching circuit **to a corresponding pixel included in a pixel group arranged in the same direction as the shift register, such that all pixels in the pixel group receive a selection signal from the shift register**". Claim 5

requires that the selection signals of the respective signal transmission methods are output to "a pixel group" and that "all pixels in the pixel group receive a selection signal".

Claim 5 does not require that the selection signals are sent to the same pixel group in the first and second signal transmission methods, or that selection signals are sent to all pixels in a vertical or horizontal direction in the second signal transmission method.

Therefore, in the first signal transmission method (all-pixel read) taught by Umeda et al.

selection signals are sent to every pixel in a group comprising all pixels in the vertical

direction (figure 22A), and in the second signal transmission method (sub-sampling

read) taught by Umeda et al. selection signals are sent to every pixel in a group

comprising every other pixel in the vertical direction (figure 22C). See paragraphs

0169-0171 and 0173.

5. Applicant argues that for at least the same reasons presented above with respect to claim 5, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 35.

6. The Examiner respectfully disagrees for the same reasons stated above with respect to claim 5. A detailed explanation is given in the rejection of claim 35.

7. Therefore the rejection is maintained by the Examiner.

Claim Objections

8. The objection made to claim 15 is hereby removed in view of Applicant's response.

Claim Rejections - 35 USC § 112

9. The rejection of claim 5 under 35 U.S.C. 112 is hereby removed in view of Applicant's response.

Claim Rejections - 35 USC § 102

10. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

11. Claims 5, 18, 19, 23, 28-30 and 35-38 are rejected under 35 U.S.C. 102(b) as being anticipated by Umeda et al. (US 2002/0145669).

12. The Examiner's response to Applicant's arguments, as outlined above, is hereby incorporated into the rejection of claim 5, 18, 19, 23, 28-30 and 35-38 by reference.

Consider claim 5, Umeda et al. teaches:

A solid state imaging apparatus (figures 1 and 22A-22C), comprising:

a plurality of pixels two-dimensionally arranged in a vertical direction and a horizontal direction wherein each of the plurality of pixels has a color filter having a different color from color filters of vertically or horizontally adjacent pixels (See figures 22A-22C); and

Art Unit: 2622

a signal output circuit (figures 1 and 23) configured to perform one of two types of operations (“all-pixels output mode” and “sub-sampling mode”, figures 23, paragraphs 0169-0171),

wherein the signal output circuit includes:

a shift register (vertical scanning section, 103, figure 1) for sequentially outputting selection signals, which drive each pixel, to all of the plurality of pixels either in a vertical or a horizontal direction (vertical direction, see paragraphs 0122, 0123 and 0148, figure 11B), and

an operation switching circuit (switch circuit, 101e, figure 23) for outputting the selection signals from the shift register to each pixel (The operation switching circuit (101e) controls whether the selection signals are output in an all-pixel output mode or sub-sampling mode, paragraphs 0170 and 0171, figure 23.), the operation switching circuit configured to switch between a first signal transmission method (all-pixel output mode) in which the selection signals are sequentially output to all pixels either in the vertical direction (Selection signals are output to all pixels in the vertical direction, figure 22A, paragraphs 0169 and 0171.) and a second signal transmission method (sub-sampling mode) in which the selection signals are continuously output to some pixels having color filters of the same color (i.e. green pixels) either in the vertical direction or the horizontal direction (in the vertical direction, figure 22C, paragraphs 0169 and 0173), and

wherein in both of the first and second signal transmission methods, each of the selection signals of the shift register (103) is output via the operation switching circuit

Art Unit: 2622

(101e) to a corresponding pixel included in a pixel group arranged in the same direction as the shift register (i.e. a group of all pixels in the vertical direction in the all-pixel output mode and a group of all green pixels in the vertical direction in the sub-sampling mode), such that all pixels in the pixel group receive a selection signal from the shift register (See figures 22A and 22C, paragraphs 0169-0173. The operation switching circuit (101e) causes the shift register to output selection signals to all pixels in the all-pixel output mode and all green pixels in the sub-sampling mode.).

Consider claim 18, and as applied to claim 5 above, Umeda et al. further teaches that the first signal transmission method is a sequential scanning method, and the second signal transmission method is a pixel mixture scanning method (The first signal transmission method sequentially outputs all pixel signals and the second signal transmission method outputs a pixel mixture of only green pixels, paragraphs 0169, 0171 and 0173.).

Consider claim 19, and as applied to claim 18 above, Umeda et al. further teaches that a static image mode is executed by the sequential scanning method, and a moving image mode is executed by the pixel mixture scanning method (The sub-sampling (i.e. pixel mixture) method is used in video capture mode (i.e. moving image mode), and the all-pixel readout method is used in still image mode, paragraph 0170.).

Consider claim 23, and as applied to claim 5 above, Umeda et al. further teaches the first signal transmission method sequentially outputs all the pixel signals having color filters of the different colors from one another (Selection signals are output to all pixels in the vertical direction, figure 22A, paragraphs 0169 and 0171.).

Consider claim 28, and as applied to claim 5 above, Umeda et al. further teaches:

in the first signal transmission method (all-pixel output mode) of the two signal transmission methods, the shift register outputs the selection signals in number order (Selection signals are sequentially output to all pixels in the vertical direction, figure 22A, paragraphs 0169 and 0171. Figure 11B shows that selection signals are output in number order.), and

in the second signal transmission method (sub-sampling mode) of the two signal transmission methods, the shift register outputs the selection signals, changing the order partially (The order is changed such that selection signals are only sent to green pixels in the vertical direction, figure 22C, paragraphs 0169 and 0173).

Consider claim 29, and as applied to claim 5 above, Umeda et al. further teaches that the second signal transmission method outputs signals of all of the pixels without thinning (All of the pixels output in the second signal transmission method (i.e. the green pixels) are output without thinning (See figures 22C, paragraphs 0169 and 0173-0174.).).

Consider claim 30, and as applied to claim 5 above, Umeda et al. further teaches that the solid state imaging apparatus is a MOS type solid state imaging apparatus ("CMOS", paragraph 0123), and a MOS transistor is used in the shift register (A MOS transistor (65) is used for vertical selection, paragraph 0259, figure 89.).

Consider claim 35, Umeda et al. teaches:

A solid state imaging apparatus (figures 1 and 22A-22C), comprising:

a plurality of pixels arranged two-dimensionally wherein each of the plurality of pixels has a color filter having a different color from color filters of adjacent pixels in a row or a column (See figures 22A-22C);

a shift register (vertical scanning section, 103, figure 1) for outputting selection signals, which drive each pixel, to a single line pixel group (i.e. a single line group of all pixels in the vertical direction in the all-pixel output mode and a single line group of all green pixels in the vertical direction in the sub-sampling mode) of the plurality of pixels (see paragraphs 0122, 0123 and 0148, figures 11B, 22A and 22C); and

an operation switching circuit (switch circuit, 101e, figure 23) for switching between two signal transmission methods when outputting the selection signals from the shift register to the single line pixel group (The operation switching circuit (101e) controls whether the selection signals are output in an all-pixel output mode or sub-sampling mode, paragraphs 0170 and 0171, figure 23.),

wherein in the first signal transmission method (all-pixel output mode) of the two signal transmission methods, the operation switching circuit outputs the selection signals without changing an order of the selection signals (Selection signals are sequentially output to all pixels in the vertical direction by the shift register (103) under control of the operation switching circuit (101e), figure 22A, paragraphs 0169 and 0171. Figure 11B shows that selection signals are output without changing an order of the selection signals.), and

in the second signal transmission method (sub-sampling mode) of the two signal transmission methods, the operation switching circuit outputs the selection signals, changing the order of the selection signals partially (The order is changed such that selection signals are only sent to green pixels in the vertical direction by the shift register (103) under control of the operation switching circuit (101e), figure 22C, paragraphs 0169 and 0173), and

in both of the first and second signal transmission methods, each of the selection signals of the shift register (103) is output via the operation switching circuit (101e) to a corresponding pixel included in the single line pixel group (i.e. the group of all pixels in the vertical direction in the all-pixel output mode and the group of all green pixels in the vertical direction in the sub-sampling mode), such that all pixels in the single line pixel group receive a selection signal from the shift register (See figures 22A and 22C, paragraphs 0169-0173. The operation switching circuit (101e) causes the shift register to output selection signals to all pixels in the all-pixel output mode and all green pixels in the sub-sampling mode.).

Consider claim 36, and as applied to claim 35 above, Umeda et al. further teaches that the first signal transmission method (all-pixel output mode) provides a first operation outputting all of the pixels included in the single line pixel group (Selection signals are sequentially output to all pixels in the vertical direction, figure 22A, paragraphs 0169 and 0171. Figure 11B shows that selection signals are output in number order.), and

the second signal transmission method (sub-sampling mode) provides a second operation continuously outputting some of the pixels included in the single line pixel group and having color filters of a same color (The order is changed such that selection signals are sent to all pixels in the green pixel group in the vertical direction, figure 22C, paragraphs 0169 and 0173).

Consider claim 37, and as applied to claim 35 above, Umeda et al. further teaches that the second signal transmission method (sub-sampling mode) outputs signals of all of the pixels included in the single line pixel group without thinning (All of the pixels output in the second signal transmission method (i.e. the green pixels) are output without thinning (See figures 22C, paragraphs 0169 and 0173-0174.)).

Consider claim 38, and as applied to claim 35 above, Umeda et al. further teaches that the solid state imaging apparatus is a MOS type solid state imaging

Art Unit: 2622

apparatus ("CMOS", paragraph 0123), and a MOS transistor is used in the shift register (A MOS transistor (65) is used for vertical selection, paragraph 0259, figure 89.).

Claim Rejections - 35 USC § 103

13. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

14. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Umeda et al. in view of Akimoto et al. (US 5,016,108).

Consider claim 21, and as applied to claim 5 above, Umeda et al. teaches that the solid state imaging apparatus is of a MOS type ("CMOS", paragraph 0123).

However, Umeda et al. does not explicitly teach that the operation switching circuit comprises a plurality of MOS transistors selected by a plurality of signal gate lines.

Akimoto et al. similarly teaches of an MOS imager (figure 3, column 3, lines 40-43).

However, in addition to the teachings of Umeda et al., Akimoto et al. teaches that the scanning and selecting of pixel signals involves a plurality of MOS transistors (MOS transistor switches, 105, 106, 205, 206, etc.) selected by a plurality of signal gate lines (gate lines, 512, 513), column 3, line 50 through column 4, line 16.

Therefore, it would have been obvious to a person having ordinary skill in the art to include a plurality of MOS transistors selected by a plurality of signal gate lines as

Art Unit: 2622

taught by Umeda et al. as part of the operation switching circuit taught by Akimoto et al. for the benefit of enabling the scanning of selected signal lines while preventing leakage current, noise and the loss of signal charge (Akimoto et al., column 2, lines 16-27).

Allowable Subject Matter

15. Claim 15 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

16. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record teaches all of the limitation of claim 5 (see above rationale). However, the prior art of record does not teach nor reasonably suggest, as a whole, that the second signal transmission method repeats, after continuously outputting signals of the plurality of pixels having color filters of the same color, an operation which continuously outputs signals of the plurality of pixels having color filters of a different color, on a basis of a pixel mixture unit consisting of a plurality of pixels, and the pixel mixture unit consists of 25 pixels arranged in five rows and five columns.

Conclusion

17. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Art Unit: 2622

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALBERT H. CUTLER whose telephone number is (571)270-1460. The examiner can normally be reached on Mon-Thu (9:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on (571) 272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2622

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AC

/Sinh Tran/
Supervisory Patent Examiner, Art Unit 2622